

FIG. 1 is a block diagram of a system 100. The system 100 includes a processor 102, a memory 104, and a storage device 106. The processor 102 is connected to the memory 104 and the storage device 106. The memory 104 stores data 108 and instructions 110. The storage device 106 stores data 112 and instructions 114. The system 100 is configured to execute the instructions 110 and 114 to perform the operations of the system 100.

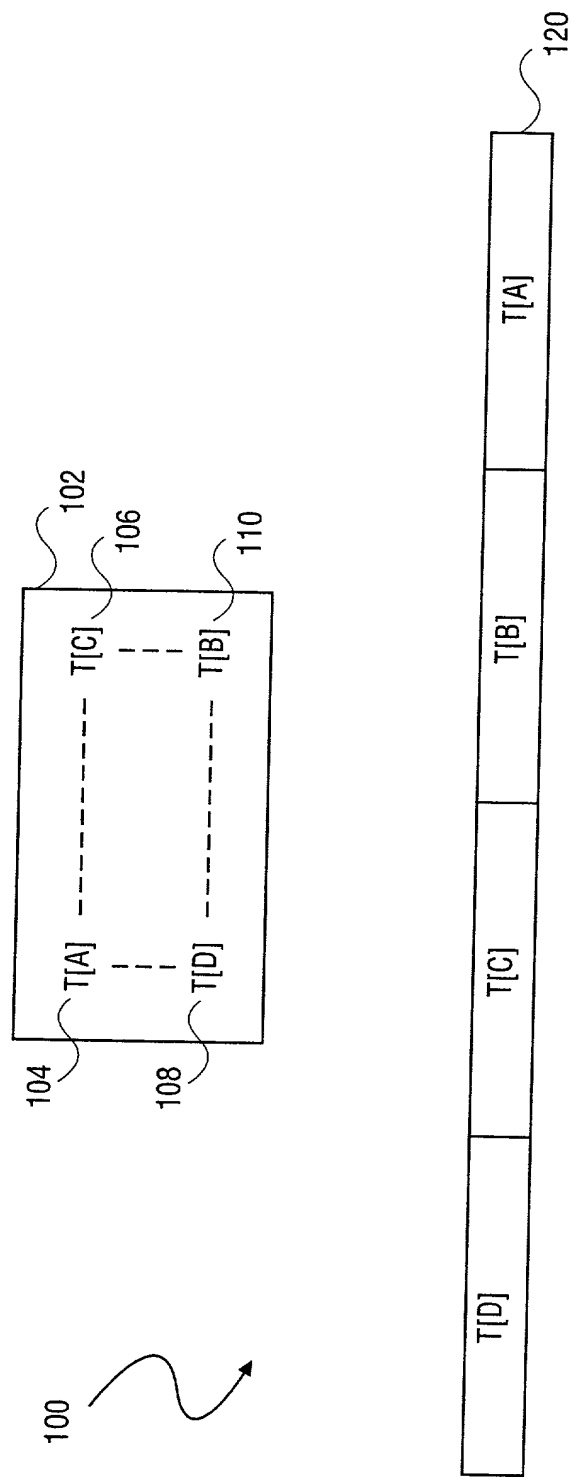


FIG. 1

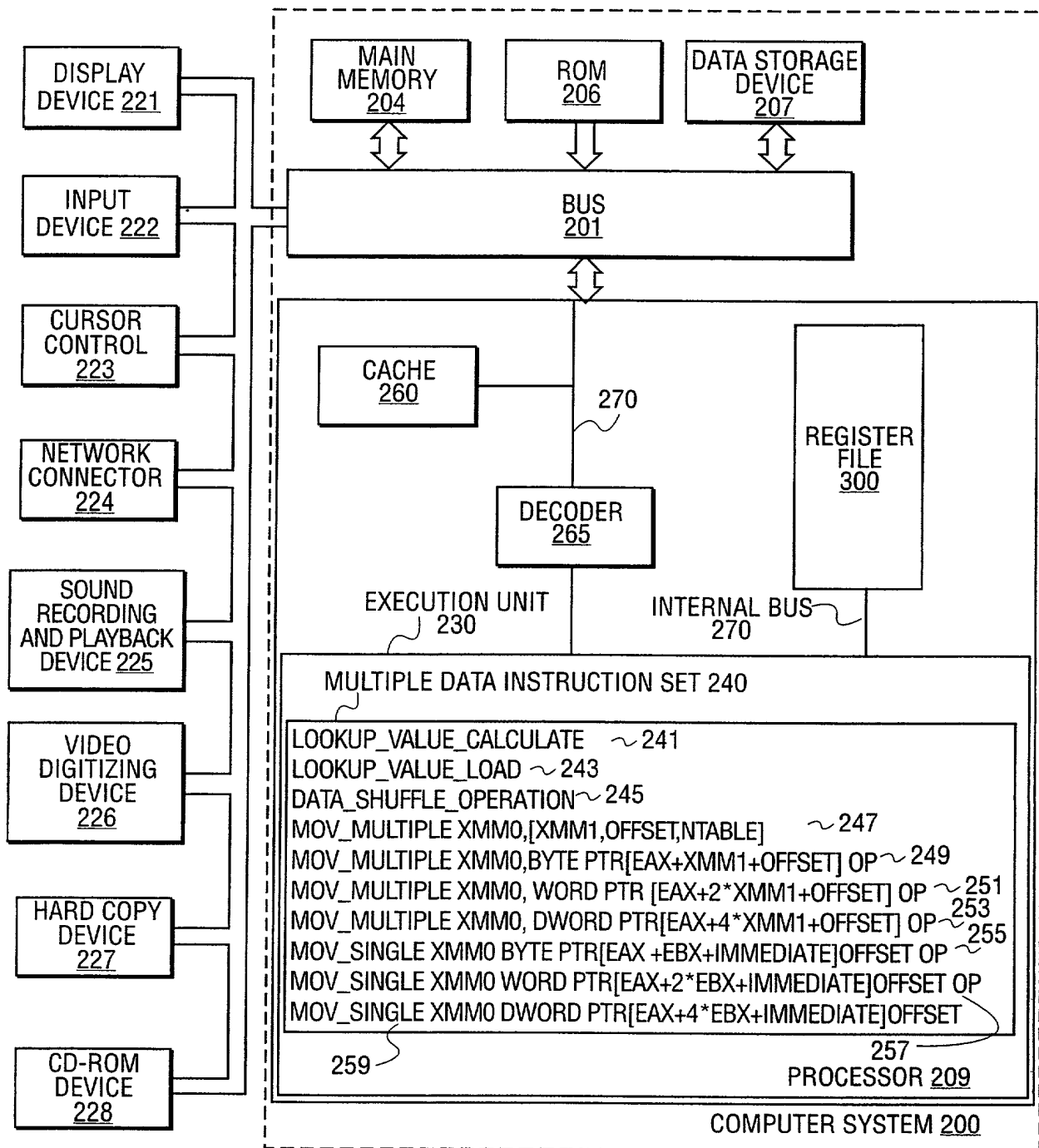
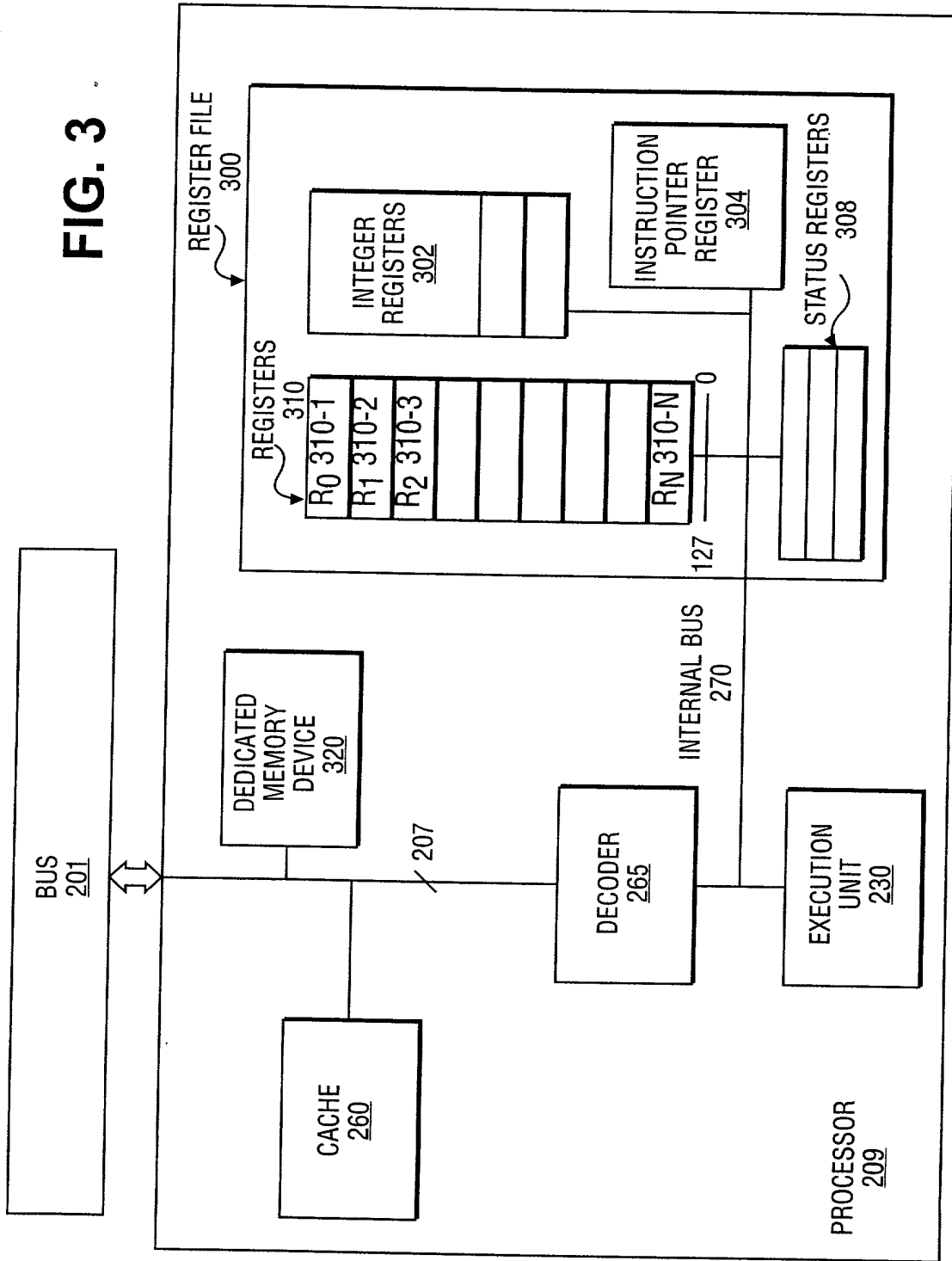
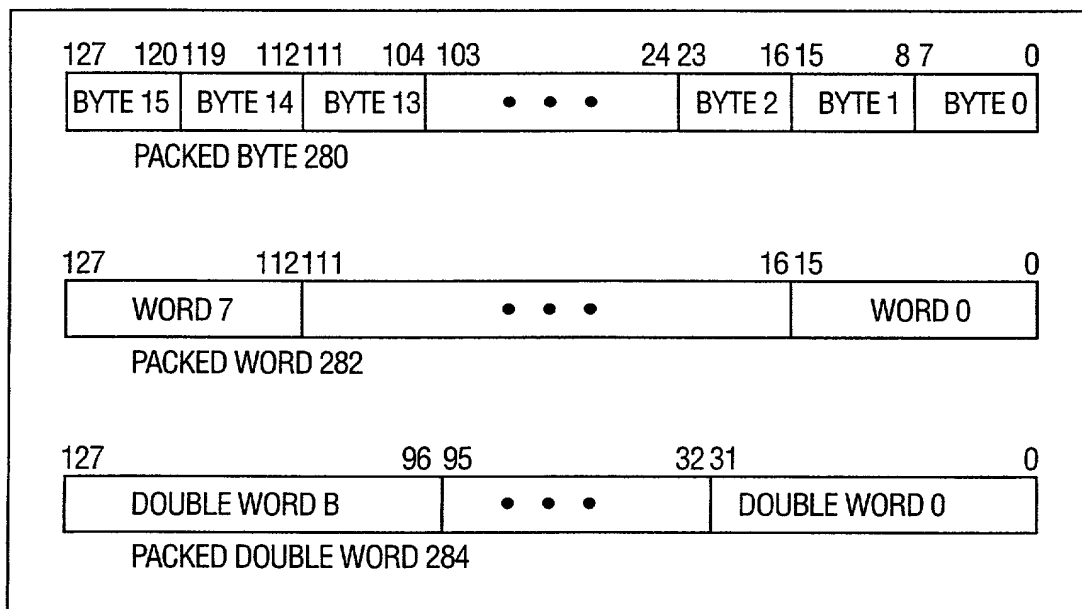


FIG. 2

FIG. 3





**FIG. 4**

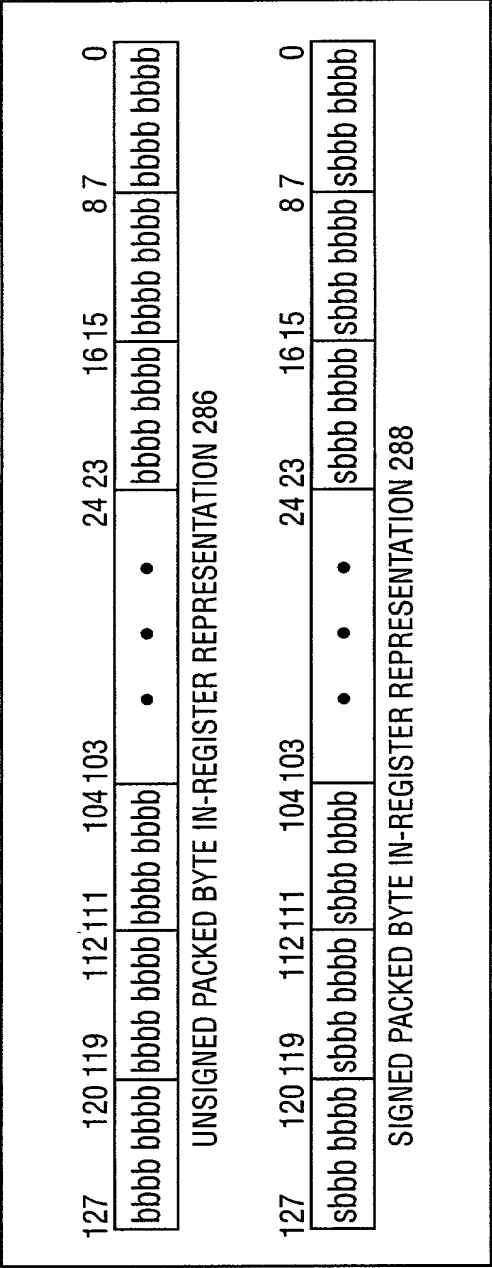


FIG. 5A

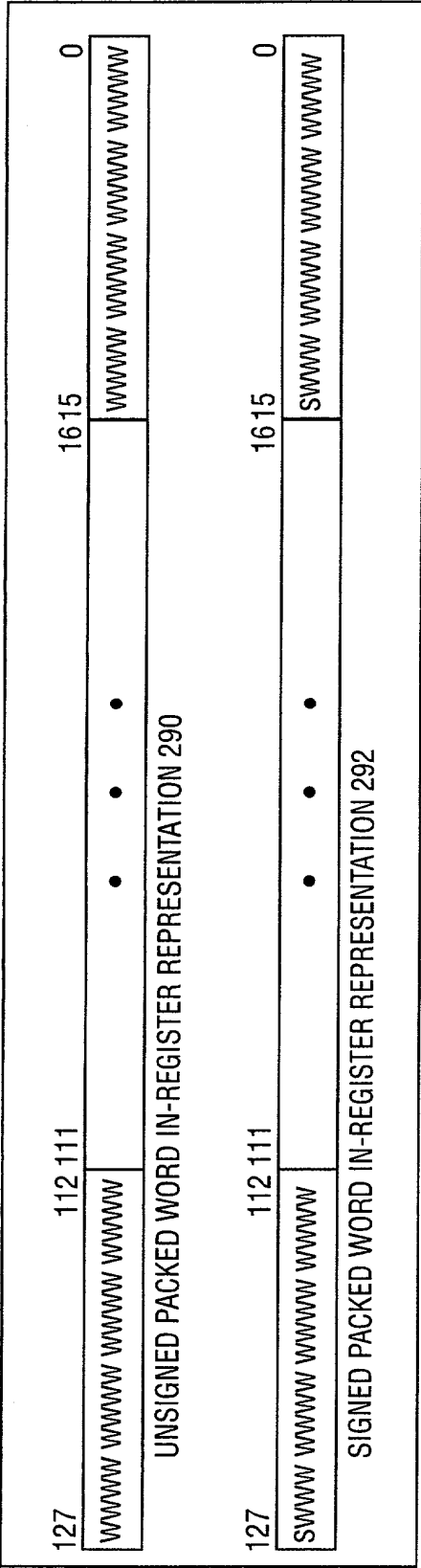


FIG. 5B

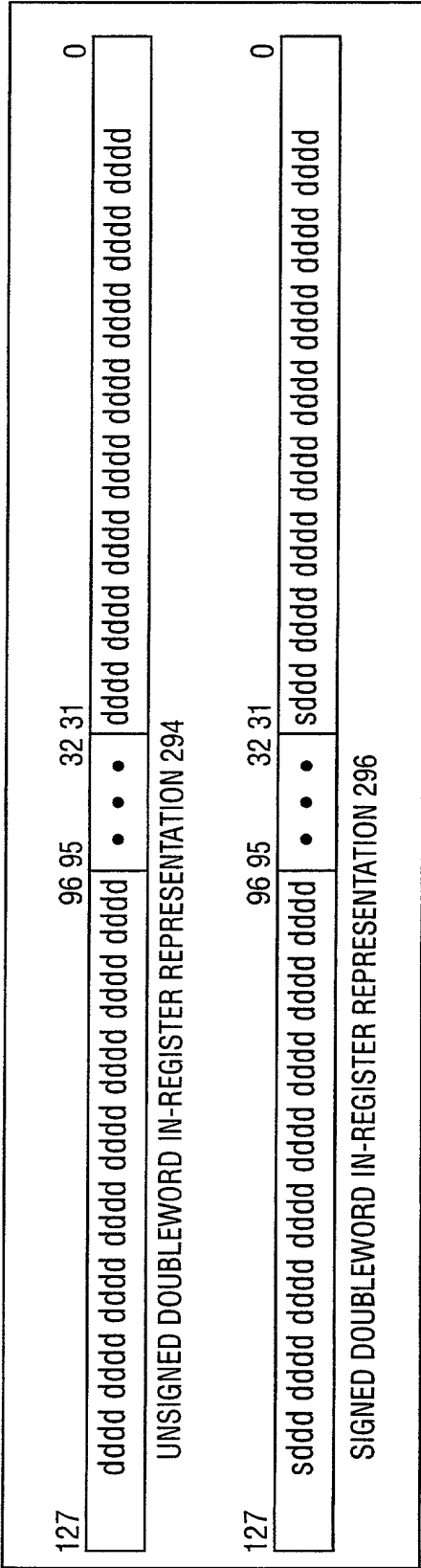


FIG. 5C

TO BUS 201

CACHE  
260

EXECUTION  
UNIT  
230

PROCESSOR  
209

FIG. 6A

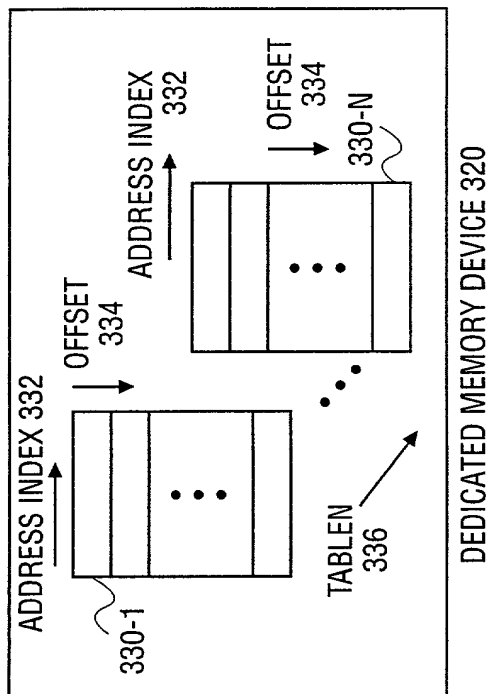
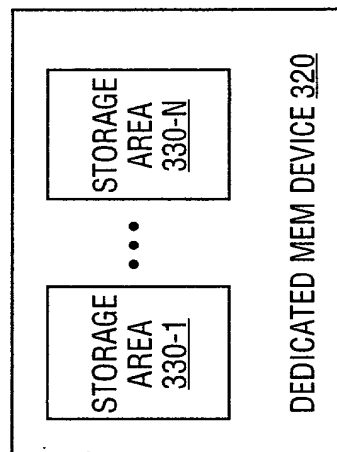


FIG. 6B

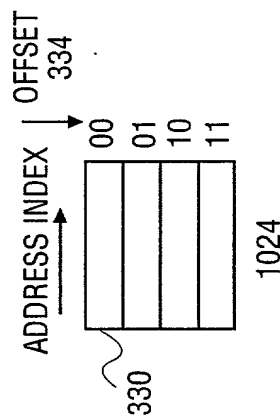
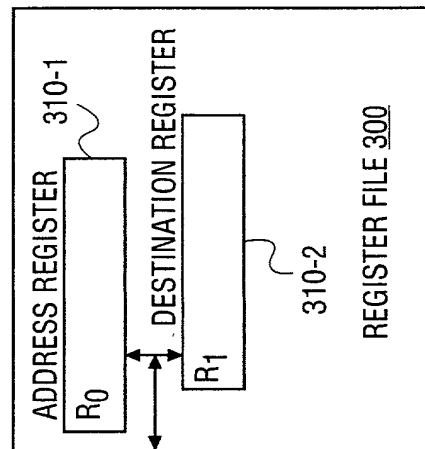


FIG. 6C

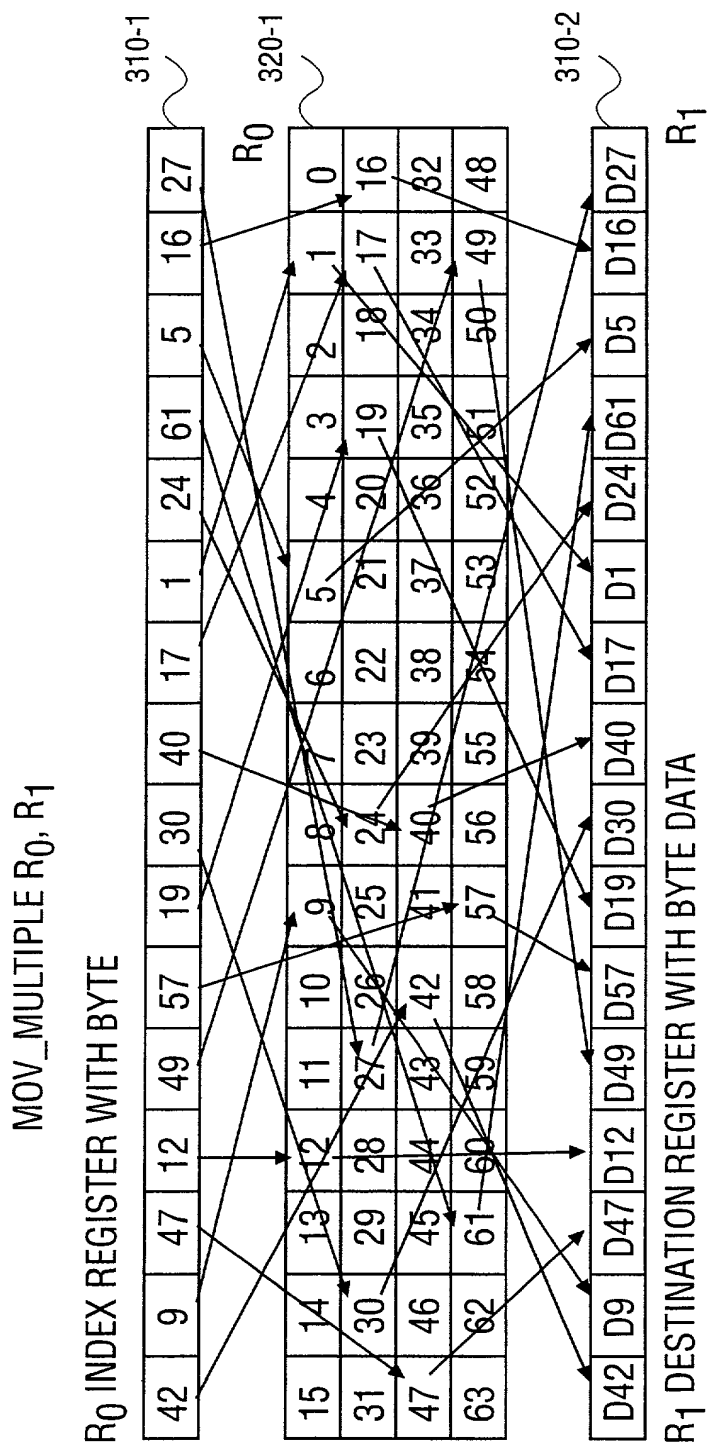


FIG. 7



MOV\_MULTIPLE R0 DWORD PTR [EAX 4 \* R1 + OFFSET]

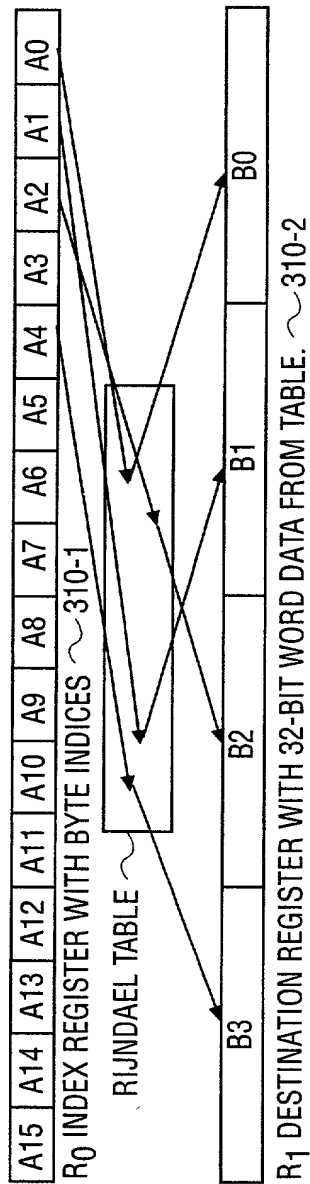


FIG. 8

310-1 ~ MOV\_MULTIPLE R0 BYTE PTR [EAX + R1 + OFFSET]  
R0 INDEX REGISTER WITH 16-BIT INDICES

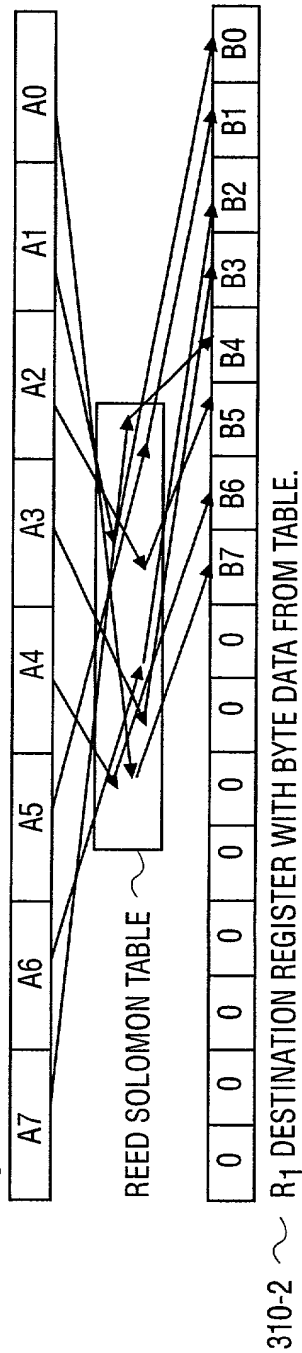


FIG. 9

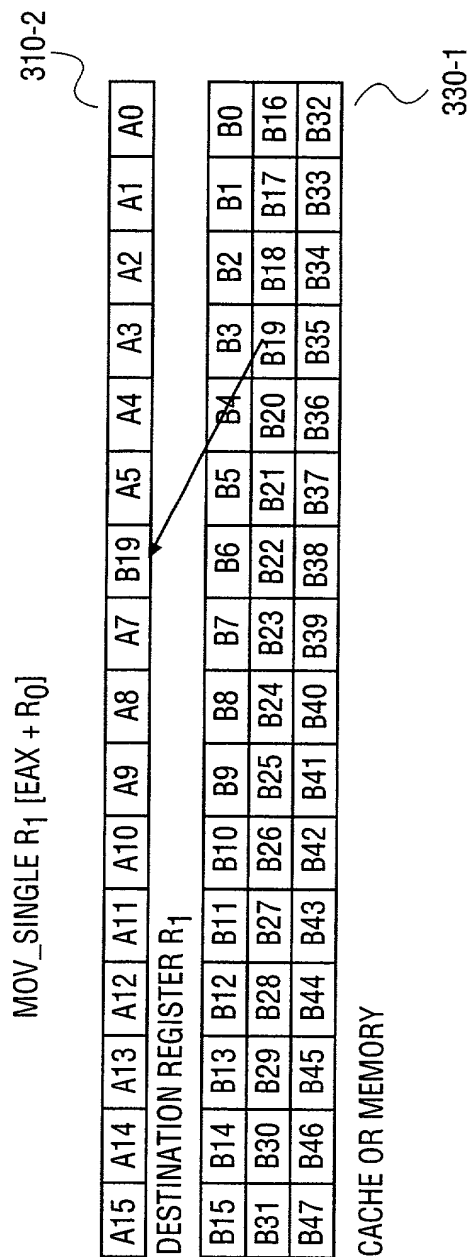


FIG. 10

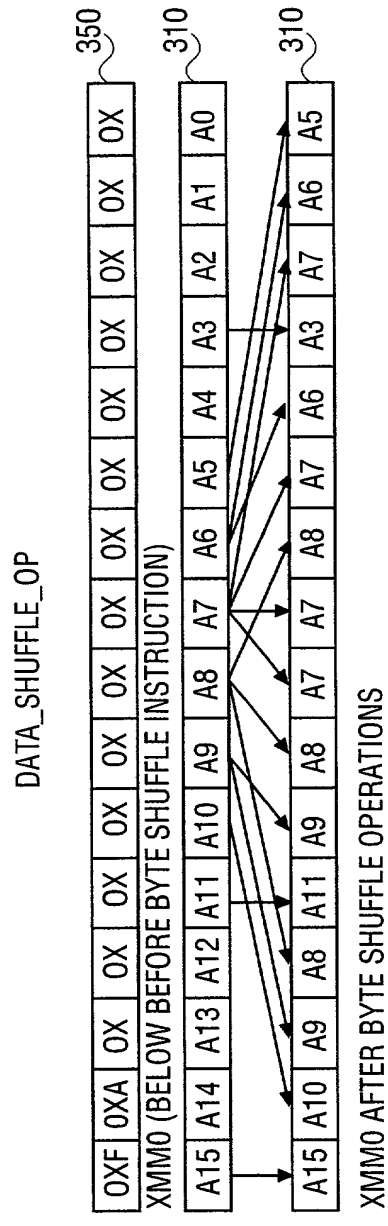
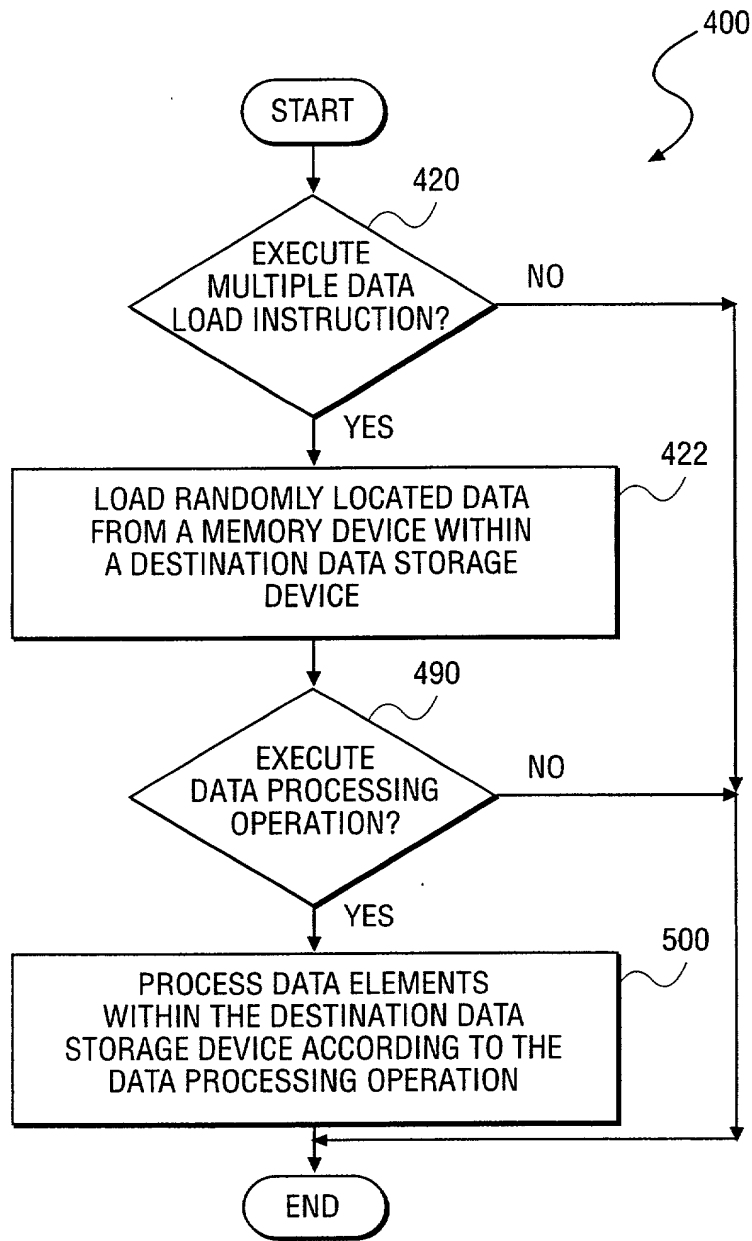
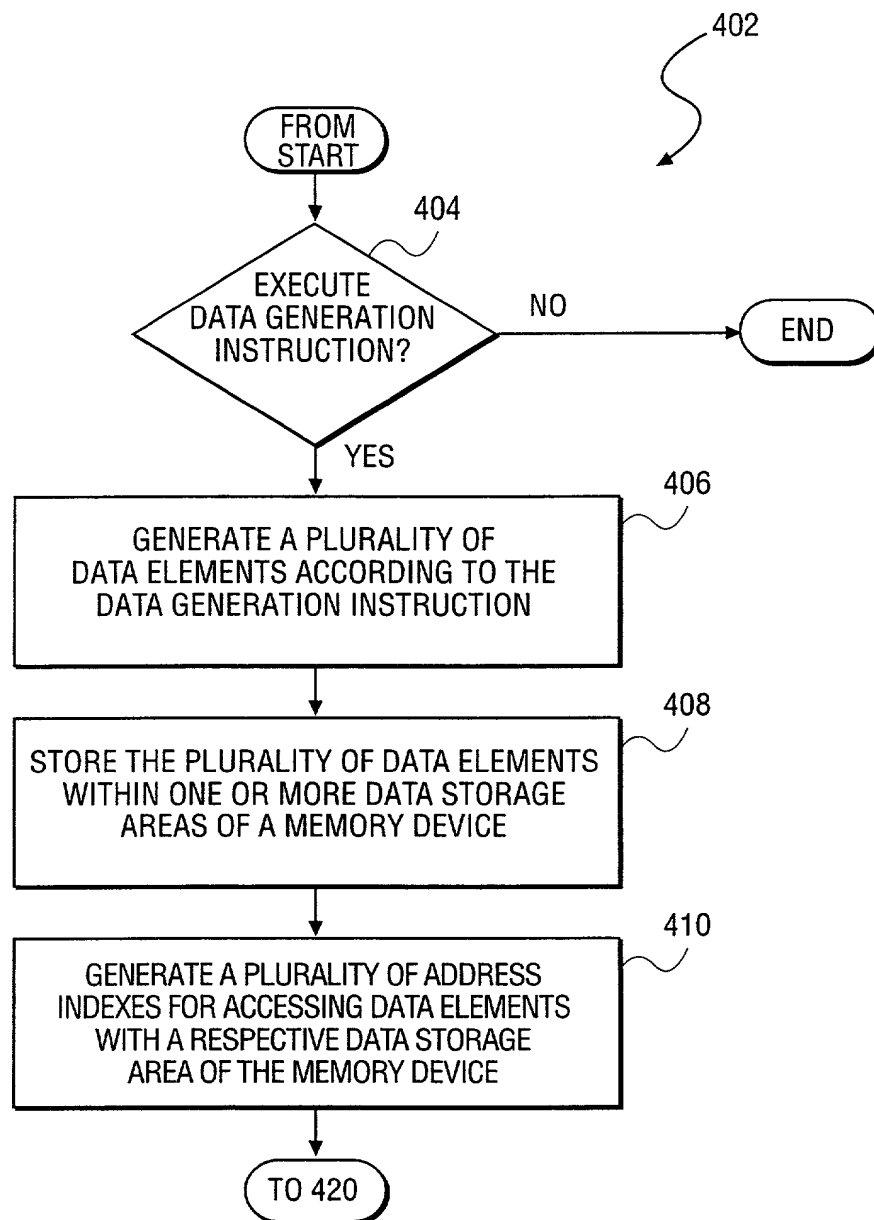


FIG. 11



**FIG. 12**



**FIG. 13**

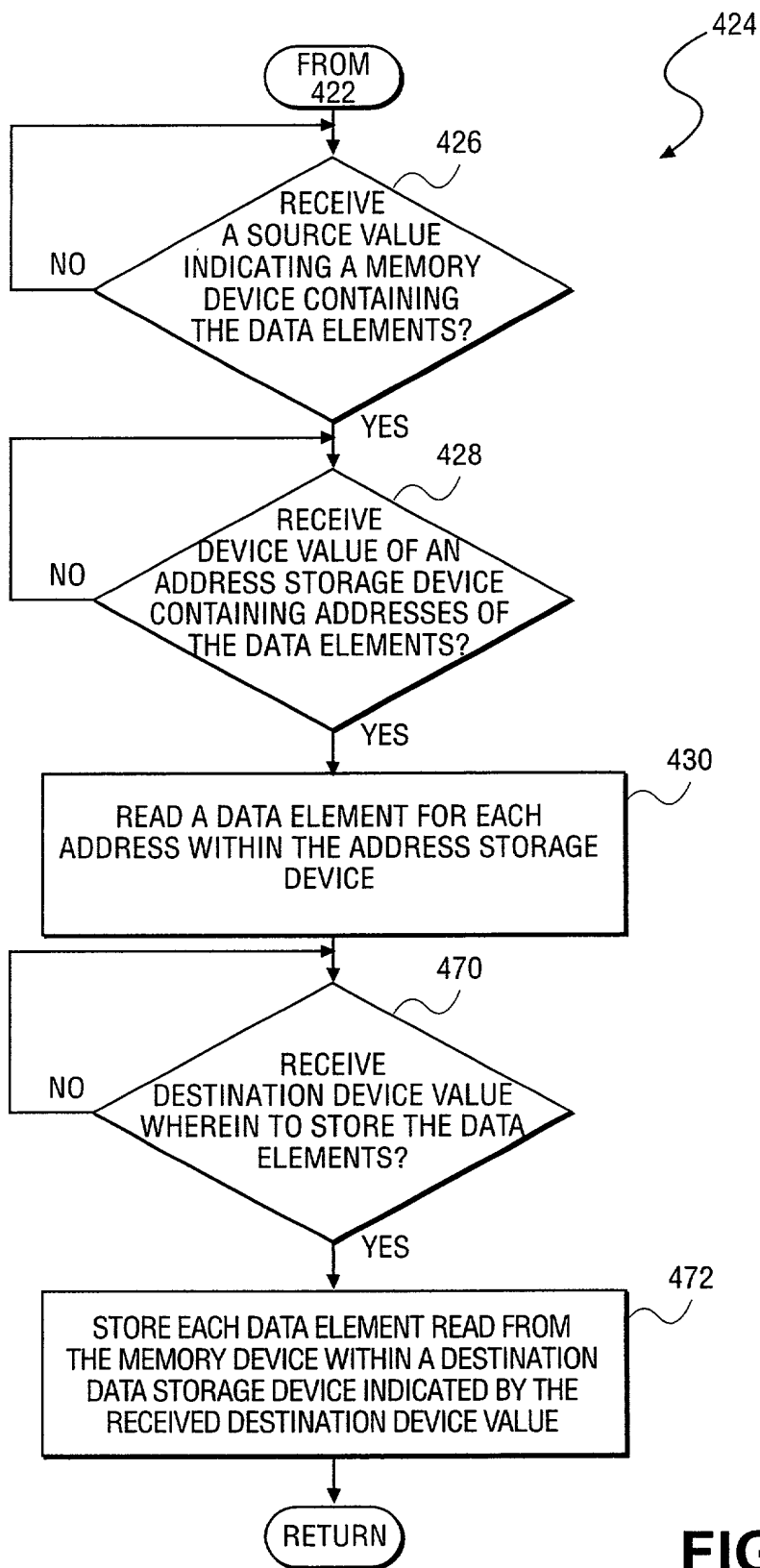
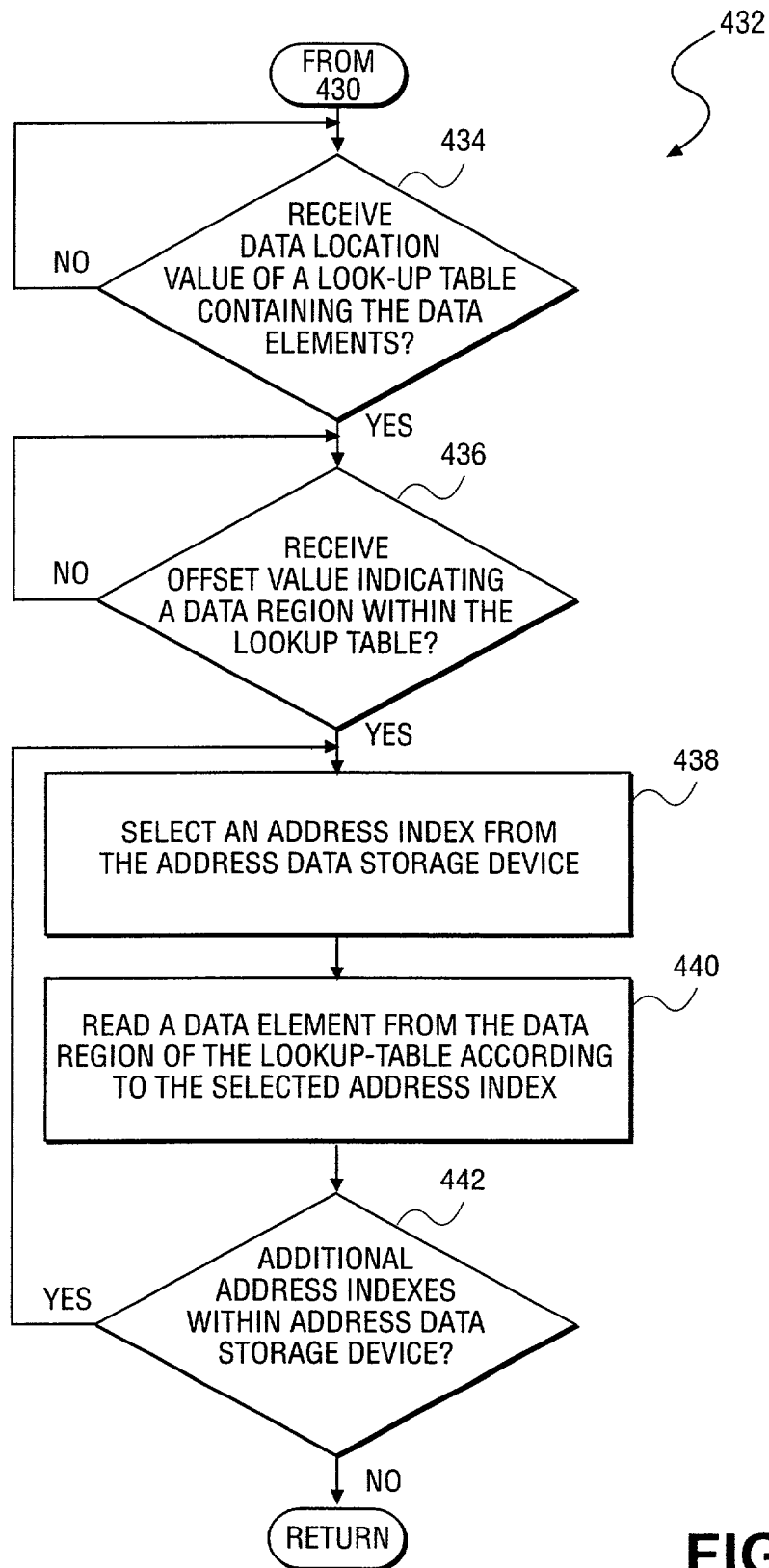


FIG. 14



**FIG. 15**

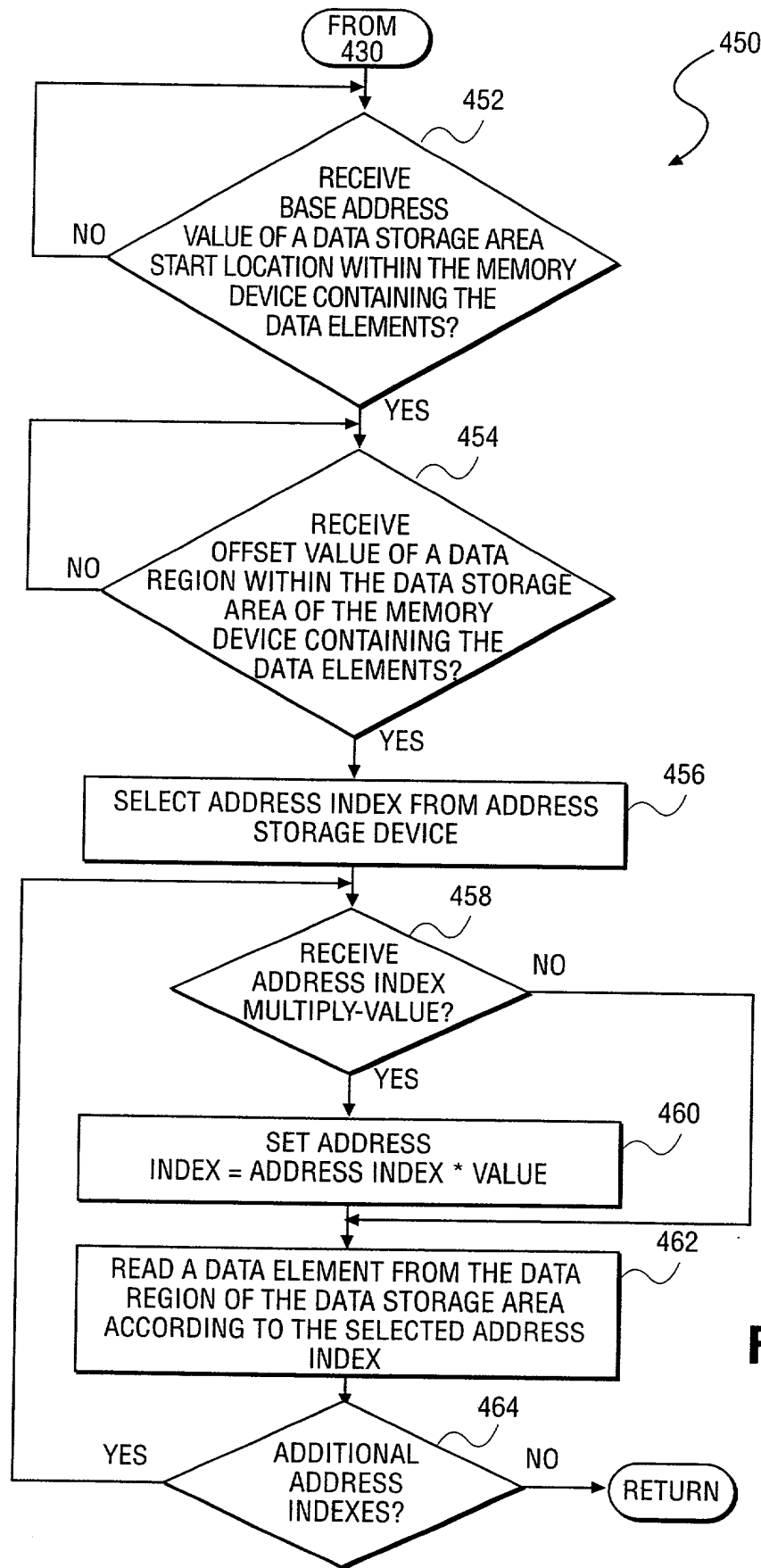


FIG. 16



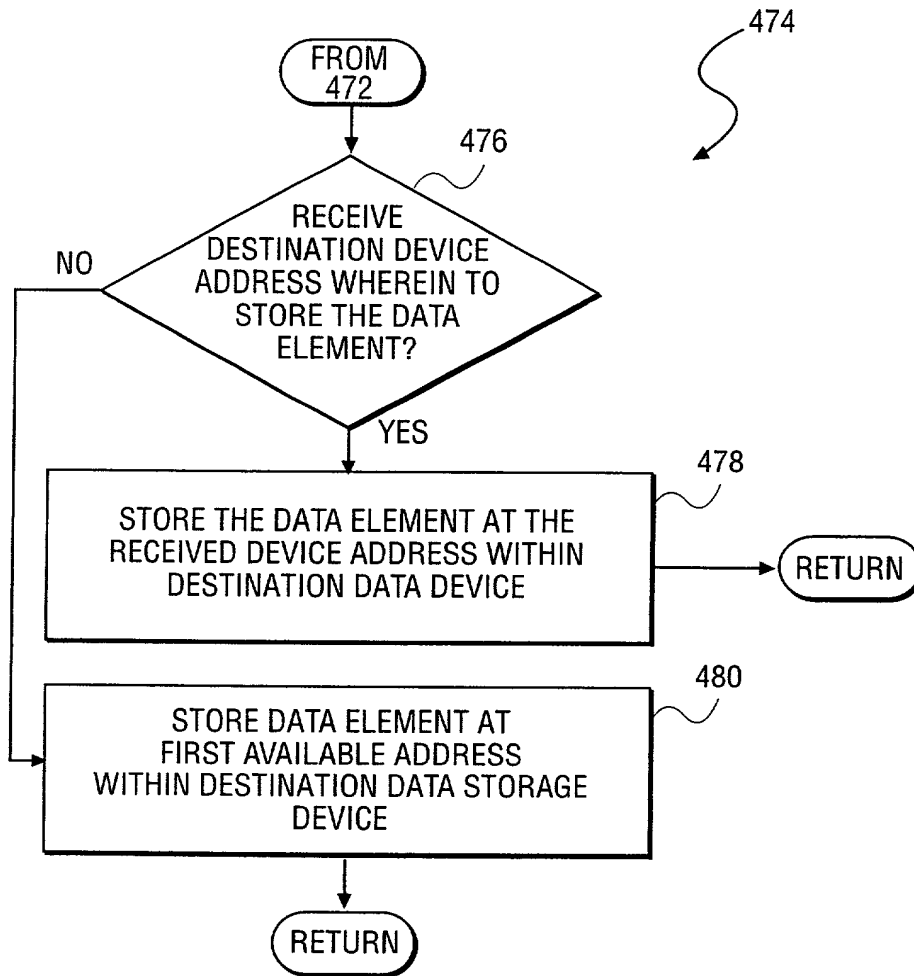


FIG. 17

